Code No.: ETCS 415 **L T C**

Paper: Advanced Computer Architecture **3 1 4**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.
2. Apart from question no. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be of 12.5 marks.

UNIT – I

Parallel computer models: The state of computing , Multiprocessors and multicomputers, Multivector and SIMD computers, Architectural development tracks

Program and network properties :Conditions of parallelism, Data and resource dependences,Hardware and software parallelism,Program partitioning and scheduling, Grain size and latency, Program flow mechanisms,Control flow versus data flow,Data flow architecture,Demand driven mechanisms,Comparisons of flow mechanisms**[No. of Hrs.: 11]**

UNIT - II

System Interconnect Architectures : Network properties and routing, Static interconnection networks, Dynamic interconnection Networks, Multiprocessor system interconnects, Hierarchical bus systems, Crossbar switch and multiport memory,Multistage and combining network.

Processors and Memory Hierarchy : Advanced processor technology, Instruction-set Architectures,CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors,VLIW Architectures, Vector and Symbolic processors

Memory Technology :Hierarchical memory technology, Inclusion, Coherence and Locality, Memory capacity planning, Virtual Memory Technology **[No. of Hrs.: 11]**

UNIT - III

Backplane Bus System: Backplane bus specification, Addressing and timing protocols, Arbitration transaction and interrupt, Cache addressing models, Direct mapping and associative caches.

Pipelining :Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques, Arithmetic Pipeline Design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipelines **[No. of Hrs. 11]**

UNIT - IV

Vector Processing Principles : Vector instruction types, Vector-access memory schemes.

Synchronous Parallel Processing : SIMD Architecture and Programming Principles, SIMD Parallel Algorithms, SIMD Computers and Performance Enhancement **[No. of Hrs.: 11]**

TEXT BOOKS:

1. Kai Hwang, “Advanced computer architecture”; TMH, 2000.

REFERENCES BOOKS:

1. J.P.Hayes, “computer Architecture and organization”, MGH, 1998.
2. M.J Flynn, “Computer Architecture, Pipelined and Parallel Processor Design”, Narosa Publishing, 1998.
3. D.A.Patterson, J.L.Hennessy, “Computer Architecture :A quantitative approach”, Morgan

Kauffmann, 2002.
4. Hwang and Briggs, “ Computer Architecture and Parallel Processing”; MGH, 2000.