Date: 11/02/15

BATCH: 4th Sem IT

COMPUTER ARCHITECTURE AND ORGANIZATION (ETCS-204)

ASSIGNMENT-1

Submission Date: 16/02/15

M.M: 30 marks

Q.1: Give the two's complements of the following values. Each number is represented as an 8-bit value.

a) 64

b) 33

c) -1

[3 marks]

Q.2: Show the representation of the following values in unsigned non-negative notation and unsigned two's complement notation. Each no. is 8-bits.

a) 29

b) -128

c) 199

[3 marks]

Q.3: Show the representation of the following values in signed-magnitude notation and signed-two's complement notation. Including the sign bit, each number has a total of 8 bits.

a) -63

b) 147

c) 85

[3 marks]

Q.4: What is the result of the following operations on unsigned non-negative numbers?

(a) 10110100 - 01110111 (b) 00111000 + 11001101 (c) 10001011 + 01110100

(d) 01110100

[4 marks]

Q.5: What is the result of the following operations on unsigned two's complement numbers?

(a) 10110100 − 01110111 (b) 0011 1000 + 1100 1101

(c) 1000 1011 + 0111 0100 (d) 01110100 − 10001011

[4 marks]

Q.6: For numbers in unsigned two's complement notation, show that adding two numbers with different signs always produces a valid result.

[2 marks]

Q.7: Show the block diagram of the hardware that implements the following register transfer statement:

$$yT_2: R2 \leftarrow R1,\quad R1 \leftarrow R2$$

[3 marks]

Q.8: Explain the IEEE 754 floating point standard.

[4 marks]

Q.9: Represent the following conditional control statement by two register transfer statements with control functions.

If (P = 1) then (R1 ← R2) else if (Q = 1) then (R1 ← R3).

[2 marks]

Q.10. Briefly explain the Arithmetic and Logic microoperations.

[2 marks]

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