VLSI DESIGN

Paper Code: ETIC-414	**L**	**T/P**	**C**
Paper: VLSI Design	**3**	**0**	**3**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.
2. Apart from Q. No. 1 rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be of 12.5 marks.

Objective: The prerequisite are analog devices, STLD, Digital system design and micro-electronics. The students are introducing to MOS technology, design rules and some applications.

UNIT I

Evolution of VLSI, MOS transistor theory, MOS structure, enhancement & depletion transistor, threshold voltage, MOS device design equations, MOSFET scaling and small geometry effects, MOSFET capacitances.
NMOS inverter, CMOS inverter, DC characteristics, static load MOS inverter, pull up/pull down ratio, static & dynamic power dissipation, CMOS & NMOS process technology – explanation of different stages in fabrication, body effect, latch up in CMOS.

[T1,T2][No. of Hours: 11]

UNIT II

Stick diagram and design rules, lambda based design rules, switching characteristics & inter connection effects: rise time, fall time delays, noise margin.
CMOS logic gate design: NAND, NOR, XOR and XNOR gates, Transistor sizing, combinational MOS logic circuits: pass transistor and transmission gate designs, Pseudo NMOS logic.

[T1,T2][No. of Hours: 11]

UNIT III

Sequential MOS logic circuits: SR latch, clocked latch and flip flop circuits, CMOS D latch and edge triggered flip flop, dynamic logic circuits; basic principle, non ideal effects, domino CMOS logic, high performance dynamic CMOS circuits, clocking issues, clock distribution.

[T1,T2][No. of Hours: 11]

UNIT IV

VLSI designing methodology, design flow, design Hierarchy, concept of regularity, modularity & locality, VLSI design style, Design quality, computer aided design technology, adder design and multiplier design examples. Low power design concepts using CMOS Technology.

[T1,T2][No. of Hours: 11]

Text Books:

[T1] Basic VLSI Design - Pucknell Douglas A., Eshraghian Kamran, PHI Learning Pvt Limited, 2013.

[T2] N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective - 4th Edition", Pearson Education, India.

Reference Book:

[R1] S. M. Kang, Y. Lebiebici, “CMOS digital integrated circuits analysis & design” Tata McGraw Hill, 3rd Edition.

[R2] Digital Integrated Circuit Design- Ken Martin, Oxford University Press

[R3] The MOS Transistor- Yaniiis Tsividis and Colin Mcandrew, Oxford University Press, 2013

[R4] J. M. Rabaey, “Digital Integrated Circuits” PHI Learning Pvt Limited, India

[R5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., New York, NY

[R6] Neelam Sharma, "Digital Logic Design", Ashirwad Publication 2013-14